WHAT IS CLAIMED IS:

1. An input circuit for an integrated circuit device, the input circuit comprising:

a boosting circuit configured to receive a supply voltage of the integrated circuit device and to generate a boosted voltage higher than the supply voltage;

a protection circuit configured to receive an input signal and the boosted voltage and to generate an output signal that changes responsive to changes in the input signal; and

a buffer circuit configured to generate a buffered output signal responsive to the output signal generated by the protection circuit.

2. An input circuit according to Claim 1 wherein the protection circuit is configured to generate a logic high voltage level output responsive to a logic high voltage level of the input signal, wherein the protection circuit is configured to generate a logic low voltage level output responsive to a logic low voltage level of the input signal, and wherein the logic high voltage level output of the protection circuit is less than a logic high voltage level of the input signal.

3. An input circuit according to Claim 1 wherein a logic high voltage level of the output signal is less than a logic high voltage level of the input signal.

4. An input circuit according to Claim 3 wherein the protection circuit comprises a MOS transistor having a gate coupled to the boosted voltage and a first source/drain coupled to the input signal, wherein the output signal is generated at a second source/drain of the MOS transistor, and wherein high voltage level of the output signal is approximately a difference between the boosted voltage and a threshold voltage of the MOS transistor.

5. An input circuit according to Claim 1 wherein the boosting circuit is configured to generate the boosted voltage having a voltage approximately two times higher than the supply voltage.

6. An input circuit according to Claim 1 wherein the boosting circuit comprises a charge pump.

7. An input circuit according to Claim 1 wherein the protection circuit comprises a pass transistor having a control electrode coupled to the boosted voltage, an input electrode coupled to the input signal, and an output electrode, wherein the output signal is generated at the output electrode and wherein the output signal is approximately equal to a difference between the boosted voltage and a threshold voltage of the pass transistor.

8. An input circuit according to Claim 1 wherein the buffer circuit includes first and second serially coupled switching circuits, wherein the first switching circuit inverts the output signal generated by the protection circuit and wherein the second switching circuit inverts the output of the first switching circuit to generate the buffered output signal.

9. An input circuit according to Claim 8 wherein the first switching circuit comprises first and second transistors serially coupled between the supply voltage and ground.

10. An input circuit according to Claim 9 wherein the second switching circuit comprises third and fourth transistors serially coupled between the supply voltage and ground.

11. An input circuit according to Claim 10 wherein the third transistor comprises a PMOS transistor having a gate electrically coupled to an output of the first switching circuit.

12. An input circuit according to Claim 11 wherein the fourth transistor comprises an NMOS transistor having a gate electrically coupled to the output of the first switching circuit and wherein the fourth transistor is electrically coupled in series between the third transistor and ground.

13. An input circuit according to Claim 9 wherein the first transistor comprises a PMOS transistor having a gate electrically coupled to an output of the protection circuit.

14. An input circuit according to Claim 13 wherein the second transistor comprises an NMOS transistor having a gate electrically coupled to the output of the protection circuit and wherein the second transistor is electrically coupled in series between the first transistor and ground.

15. An input circuit according to Claim 1 wherein the boosting circuit includes a supply voltage boosting circuit configured to boost a level of the supply voltage and a supply voltage dropping circuit configured to drop a level of the supply voltage.

16. An input circuit according to Claim 1 wherein the boosting circuit comprises:

a first PMOS transistor electrically coupled in series with a first NMOS transistor between the supply voltage and an output of the boosting circuit wherein the first NMOS transistor is between the first PMOS transistor and the supply voltage;

a second PMOS transistor electrically coupled in series with a second NMOS transistor between the supply voltage and an output of the boosting circuit

wherein the second NMOS transistor is between the second PMOS transistor and the supply voltage;

a first capacitor coupled to a bulk of the first and second PMOS transistors;

a second capacitor coupled to a source terminal of the first NMOS transistor and to a gate terminal of the second NMOS transistor;

a third capacitor coupled to a source terminal of the second NMOS transistor and to a gate terminal of the first NMOS transistor; and

a fourth capacitor coupled to the output of the boosting circuit.

17. An input circuit according to Claim 1 wherein the protection circuit comprises a pass transistor having a gate coupled to the boosted voltage of the boosting circuit, a first source/drain coupled to the input signal, and a second source/drain coupled to the buffer circuit.

18. An input circuit according to Claim 17 wherein the pass transistor comprises an NMOS transistor.

19. An input circuit according to Claim 1 wherein a logic high voltage level of the input signal is greater than approximately 4.5 volts and wherein the supply voltage of the integrated circuit device is less than approximately 2 volts.

20. An input circuit according to Claim 1 wherein the buffer circuit comprises two serially coupled inverters.

21. An input circuit according to Claim 1 wherein a logic high voltage level of the buffered output signal is less than approximately 2 volts.

22. A method of receiving an input signal for an integrated circuit device, the method comprising:

generating a boosted voltage responsive to a supply voltage of the integrated circuit device wherein the boosted voltage is higher than the supply voltage;

generating an output signal responsive to the boosted voltage and the input signal wherein the output signal changes responsive to changes in the input signal; and

generating a buffered output signal responsive to the output signal.

23. A method according to Claim 22 wherein generating the output signal comprises:

generating a logic high voltage level output responsive to a logic high voltage level of the input signal wherein the logic high voltage level output is less than a logic high voltage level of the input signal; and

generating a logic low voltage level output responsive to a logic low voltage level of the input signal.

24. A method according to Claim 22 wherein a logic high voltage level of the output signal is less than a logic high voltage level of the input signal.

25. A method according to Claim 22 wherein generating the boosted voltage responsive to the supply voltage comprises generating the boosted voltage to have a voltage approximately two times higher than the supply voltage.

26. A method according to Claim 22 wherein generating the boosted voltage comprises generating the boosted voltage using a charge pump.

27. A method according to Claim 22 wherein a logic high voltage level of the input signal is greater than approximately 4.5 volts and wherein the supply voltage of the integrated circuit device is less than approximately 2 volts.

28. A method according to Claim 22 wherein generating the buffered output signal comprises inverting the output signal twice.

29. A method according to Claim 22 wherein a logic high voltage level of the buffered output signal is less than approximately 2 volts.

30. A method according to Claim 22 wherein generating the output signal comprises generating the output signal using a transistor having a control electrode coupled to the boosted voltage, an input electrode coupled to the input signal, and an output electrode, wherein the output signal is generated at the output electrode and wherein the output signal is approximately equal to a difference between the boosted voltage and a threshold voltage of the transistor.